Tanzania Journal of Engineering and Technology 2025, **44**(2):41-50
OPEN ACCESS articles distributed under Creative Commons Attribution License [CC BY-ND]
Websites: https://ajol.org/tjet; https://tjet.udsm.ac.tz

ISSN 1821-536X (**print**); ISSN 2619-8789 (**electronic**)
https://doi.org/10.52339/tjet.v44i2.1264

Special Issue – 8th International Conference on Mechanical and Industrial Engineering, October 24 – 25, 2024 at The Nelson Mandela African Institute of Science and Technology, Arusha - Tanzania

Analysis of an Improved Reliability Dual-Buck Structured Three-Level Flying Capacitor Inverter

Almachius Kamala Kahwa[†] and Aviti Thadei Mushi

Department of Electrical Engineering, University of Dar es Salaam, P.O. Box 35131, Dar es Salaam, Tanzania
[†]Corresponding Author: kahwa.almachius@udsm.ac.tz ; ORCID: 0000-0002-7598-1320

ABSTRACT

With the increased demand for high-reliability power converters in the electric drive-train and propulsion systems, the efforts to design and analyze converters with high fault tolerance have become apparent. Among the emerging trends to improve the reliability of power converters is the incorporation of dual-buck (DB) structures in traditional converter topologies. Thus, this paper studies a single-phase dual-buck structured three-level flying capacitor (FC) inverter. The dual-buck flying capacitor (DBFC) inverter was constructed in such a way as to suppress the shoot-through problems that may occur because of the switching mismatch and gate driver delay, as exhibited in the traditional FC inverter. The detailed operation of the DBFC inverter was performed using a comparative analysis of the traditional FC inverter as a benchmark. It was noted that the DBFC inverter considerably reduces the current stress on some switches and mitigates the shoot-through problem. Moreover, it was inferred that apart from improving the reliability of the inverter, the DBFC inverter reduces the total harmonic distortion (THD) of the output current. The 98.8% maximum efficiency and 4.03% THD were depicted in the DBFC at a switching frequency of 40 kHz. The results of the study were validated using detailed simulations and preliminary experiments.

ARTICLE INFO

1st Submitted: **Apr. 29, 2024**

Presented: **Oct. 24, 2025**

Revised: **Nov. 10, 2024**

Accepted: **Jan, 13, 2025**

Published: **June, 2025**

Keywords: *DC-AC converter, Dual-buck inverter, Flying capacitor inverter, Reliability.*

INTRODUCTION

As the demand for safer electric drive-train and propulsion systems is growing in electric vehicles, robotic systems, more-electric aircraft (MEA), and all-electric aircraft (AEA) systems, some stringent reliability and power quality constraints of the power converters are required (Ebersberger et al., 2022; Pahlevani & Jain, 2020). This demand triggers improvements in the configurations and controls of traditional power converters (Kahwa et al., 2018).

Furthermore, the demand for high-power density converters sparked the trend of replacing Si-switching devices with silicon carbide (SiC) switching devices. The adoption of SiC devices allows the converters to operate at higher switching frequencies, thereby reducing the weight and size of the filter circuit (Calderon-Lopez et al., 2020). However, this approach increases the rate of voltage (v) change over time ($\frac{dv}{dt}$) and electromagnetic interferences during the switching process that can initiate crosstalk effects between the complimentary switches of the same leg

and degrade the output power quality (Yuan et al., 2021). To mitigate this problem, among the existing solutions is injecting dead time in the complementary switches. This technique degrades the total harmonic distortion of the output voltage and current (Ning et al., 2024; Faraji et al., 2023).

The reliability improvement approach that involves constructing conventional power converters using dual-buck structures has been studied for two-level half-bridge, full-bridge, neutral-point clamped, and cascaded H-bridge converters (Khan et al., 2018; Yao, 2021). Few studies have been conducted on the flying capacitor (FC) dual-buck converters.

The circuit of the conventional three-level FC inverter is shown in Figure 1(a). The shoot-through problem exhibited by the traditional FC inverter may occur when switches Q_2 and Q_3 turn ON simultaneously (see Figure 1(b)). Such a shoot-through scenario may break switching devices as the crosstalk voltage and current increase drastically, thereby reducing the reliability of the inverter (Kahwa and Mushi, 2024).

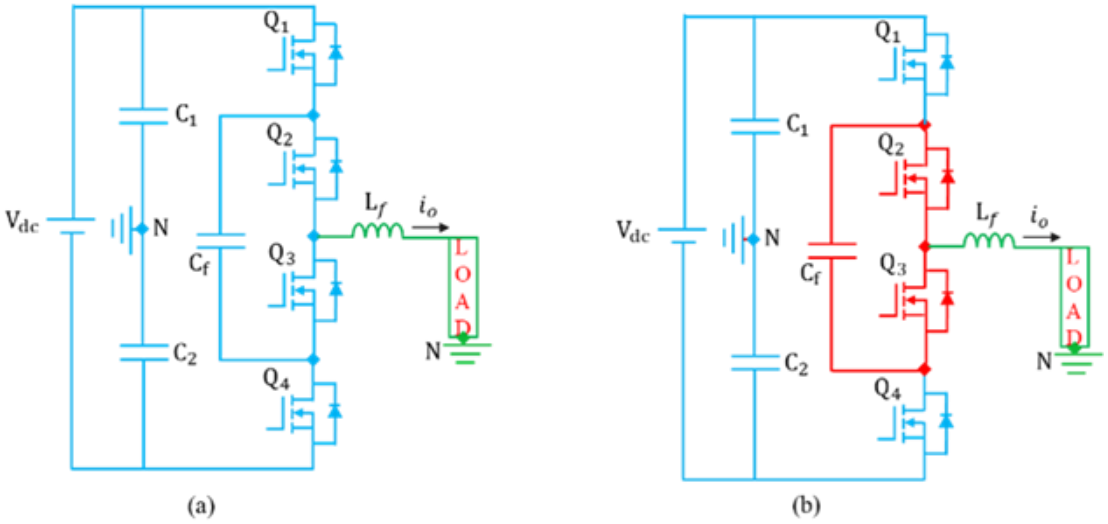

Figure 1: Single-phase three-level conventional FC inverter (a) topology and (b) shoot-through scenario.

The efforts to mitigate the shoot-through problem in the traditional three-level FC inverter were first studied by (Liu et al., 2013) and for the five-level FC inverter by (Liu et al., 2016). However, these inverter topologies require many flying capacitors and SiC diodes. The article by (Faraji et al., 2023) presented a three-level dual-buck flying capacitor inverter with fewer switching components and a capacitor that mitigates shoot-through problems. However, the voltage and current stresses across the diode are bipolar. The voltage peak-to-peak magnitude equals the whole DC source voltage, increasing the total withstand voltage and power loss. On the other hand, their manuscripts did not study the detailed theoretical analysis of the inverter in the voltage stress and shoot-through inductor design criteria.

Thus, this paper studies a novel three-level dual-buck FC inverter with reduced switching devices and flying capacitors that suppresses the shoot-through problem. The detailed comparative analysis was performed using a conventional FC inverter as a benchmark.

METHODS AND MATERIALS

Description of the Inverter Configuration

The studied novel dual-buck FC (DBFC) inverter was constructed from the

traditional three-level FC inverter shown in Figure 1 (a). The DBFC inverter topology is powered by a single DC source of magnitude V_{dc} and requires four SiC MOSFETs, one flying capacitor C_f, two dc-link capacitors, and incorporates the shoot-through protection structure, which comprises two shoot-through inductors L_{s1} and L_{s2}, and two diodes D_1 and D_2 (see Figure 2). The current flowing through the shoot-through inductor L_{s1} and L_{s2} are i_{l1} and i_{l2}, respectively. Moreover, the current flowing through the flying capacitor is i_{fc}. The node N is the neutral-potential point. The output voltage, V_{SN} of the novel DBFC inverter is obtained across nodes S and N. The inverter generates three voltage levels of magnitude $\frac{V_{dc}}{2}$, 0, and $-\frac{V_{dc}}{2}$. All the switching devices are operated at a high-switching frequency, similar to the conventional FC inverter.

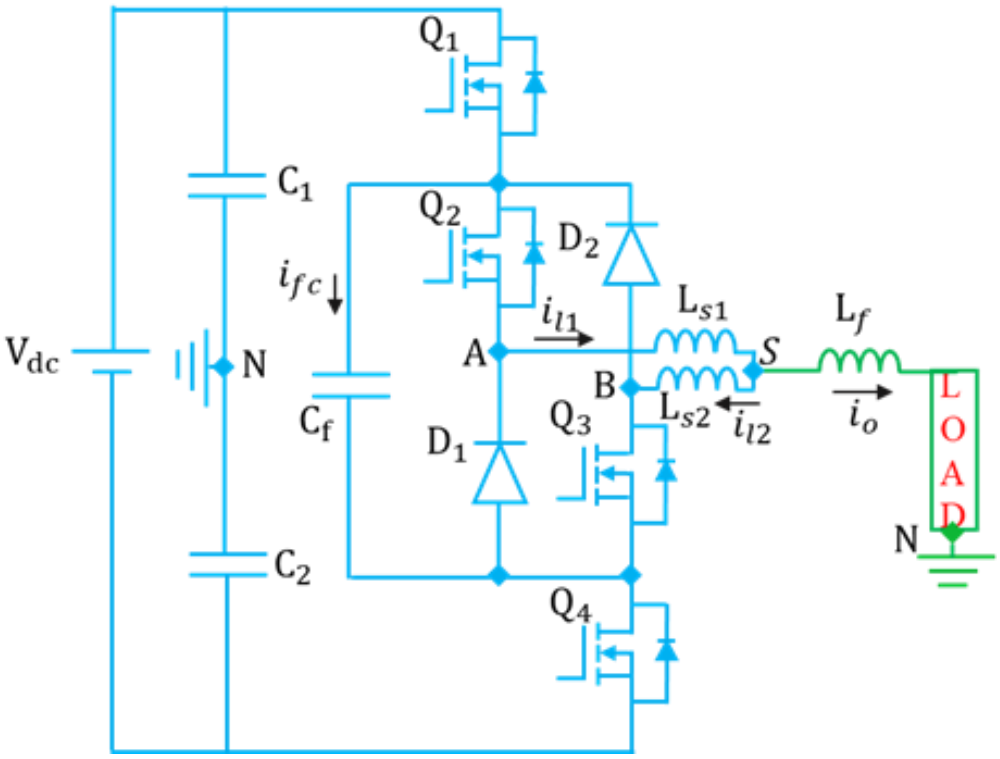

Figure 2: Novel single-phase three-level dual-buck FC inverter.

Analysis of the Inverter and its Working Principle

The output voltage of the studied novel dual-buck FC inverter is generated in four states of operation, as demonstrated in Figure 3. Under the unity power factor, the DBFC inverter in the positive half-cycle generates the output voltage using states 1 and 2 and in the negative half-cycle using states 3 and 4. The complete switching states of the three-level dual buck converter are shown in Table 1.

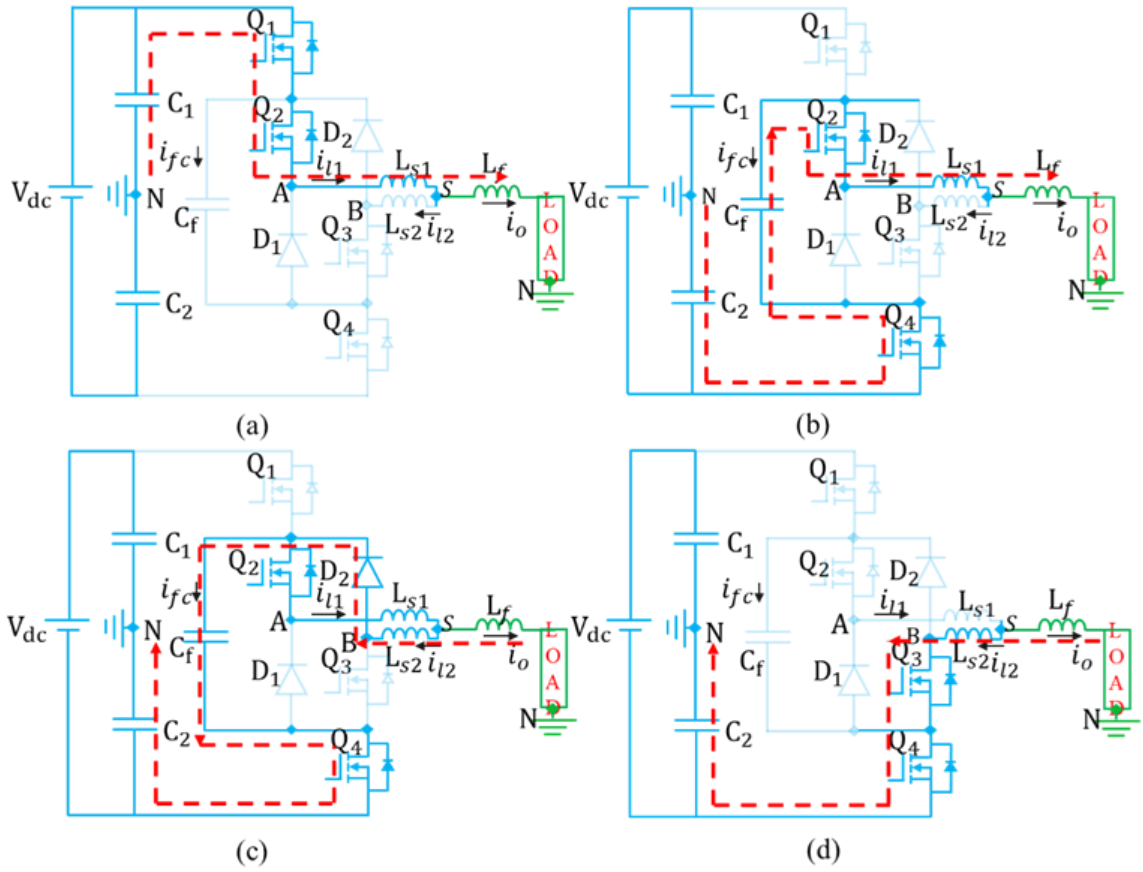

Figure 3: States of operation of the single-phase three-level dual-buck FC inverter (a) $\frac{V_{dc}}{2}$, (b) 0 V_{dc}, (c) 0 V_{dc}, and (d) $-\frac{V_{dc}}{2}$.

Table 1: Switching states of the novel three-level dual-buck FC inverter

State	Switches				Output voltage
	Q_1	Q_2	Q_3	Q_4	V_{SN}
1	1	1	0	0	$\frac{V_{dc}}{2}$
2	0	1	0	1	0
3	0	1	0	1	0
4	0	0	1	1	$-\frac{V_{dc}}{2}$

By Kirchhoff's voltage law in the DBFC inverter of Figure 2 (Kahwa and Mushi, 2024), the instantaneous shoot-through current can be obtained as

$$(L_{s1} + L_{s2})\frac{di_{sc(t)}}{dt} + i_{sc}(t)(R_{s1} + R_{s2}) = \frac{V_{dc}}{2} \quad (1)$$

where, $i_{sc}(t)$ is the instantaneous shoot-through current, t is the time during fault interval, and R_{s1} and R_{s2} are the equivalent resistances of L_{s1} and L_{s2}, respectively.
The solution to the differential equation (1) is written as

$$i_{sc}(t) = \frac{\frac{V_{dc}}{2}}{R_{s1}+R_{s2}}\left(1 - e^{-t\left(\frac{R_{s1}+R_{s2}}{L_{s1}+L_{s2}}\right)}\right). \quad (2)$$

Equation (2) was analyzed theoretically and in simulation by considering a shoot-through fault of 100 ns between switches Q_2 and Q_3 and varying the inductors from 0.1 μH to 40 μH. Other parameters

considered in this study are in Table 2. The theoretical analysis was carried out continuously in the defined range, whereas the simulation analysis was performed at discrete values within the range, as marked in Figure 4. The results of these analyses are shown in Figure 4. Both analyses confirm that the short-circuit current due to the crosstalk effect is effectively mitigated as the shoot-through inductors increase. However, the optimal short-circuit inductor design is necessary to reduce power loss in the inductor coil and its equivalent resistance.

Table 2: Parameters used in the shoot-through analysis

Parameter	Symbol	Value
DC voltage	V_{dc}	400 V
Shoot-through inductors	$L_{s1} = L_{s2}$	0.1 – 40 μH
Equivalent resistance of the shoot-through inductors	$R_{s1} = R_{s2}$	7 mΩ

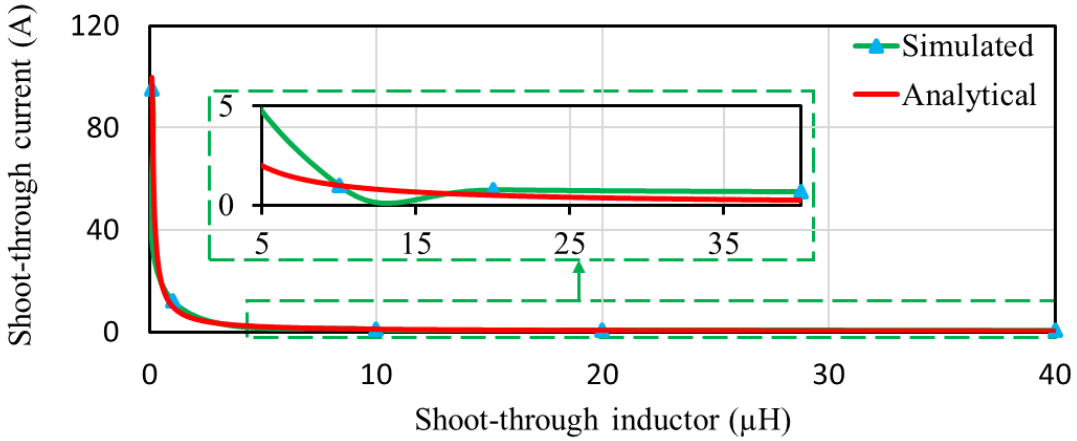

Figure 4: Shoot-through current analyzed from 0.1 μH to 40 μH of the shoot-through inductors in the novel three-level DBFC inverter.

Modulation Technique

Various modulation techniques have been developed for the conventional FC inverter. Among the available methods, phase deposition pulse-width modulation improves the harmonic content of the output voltage and current (Shukla et al., 2007). Thus, the studied novel dual-buck inverter was analyzed using a level-shifted pulse-width modulation (LS-PWM) technique based on phase deposition. The adopted LS-PWM technique compares two carrier signals of the same magnitude, phase, and frequency with the sinusoidal reference voltage signal to generate the switching signals for the switches Q_1 through Q_4. The switching signal function of Q_1 is complementary to Q_4 and that of Q_2 is complemtentary to Q_3.

Simulation Procedures and Materials

The performance analyses of the dual-buck FC inverter were simulated using the modulation strategy described in the previous subsection. This evaluation used a comparative analysis of the conventional FC inverter as a benchmark. All the simulation studies were carried out using the PLECS software environment. Both inverter topologies were analyzed using the parameters in Table 3. The output frequency of 400 Hz was considered in the analysis because it is one of the acceptable frequencies in the MEA and AEA propulsion systems.

Table 3: Simulation parameters

Parameter	Symbol	Value
DC supply voltage	V_{dc}	400 V
Shoot-through inductors	$L_{s1} = L_{s2}$	20 μH
Flying capacitor	C_f	470 μF
Load inductor	L_f	1 mH
DC-link capacitor	$C_1 = C_2$	1200 μF
Load resistor	R	19.4 Ω
Output frequency	f_o	400 Hz
Switching frequency	f_{sw}	40 kHz

RESULTS AND DISCUSSIONS

Simulation Results

The steady-state simulation results demonstrating the output voltage and current of the dual-buck FC inverter are shown in Figure 5. The generated output voltage of the inverter depicts three levels of magnitude 200, 0, and -200 V (see Figure 5 (a)), thus verifying the analysis in Table 1 and Figure 3. Moreover, the output current flowing to the load is sinusoidal with less distortion and a peak amplitude of 9.1 A (see Figure 5 (b)). These results confirm that the novel dual-buck inverter works as desired.

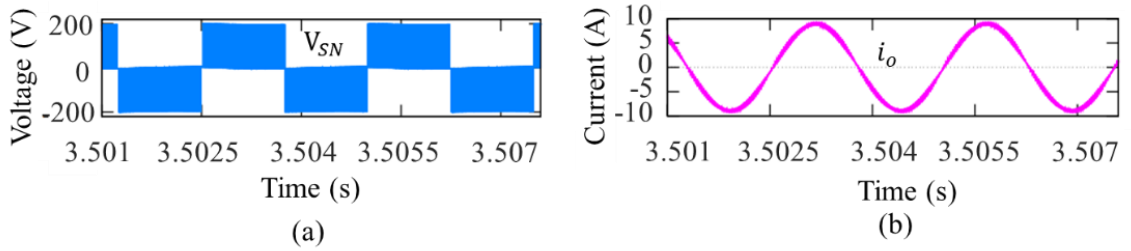

Figure 5: Simulated (a) output voltage and (b) current of the novel dual-buck FC inverter.

Furthermore, the steady-state operation performance of the novel dual-buck inverter is demonstrated in Figure 6, which depicts the flying capacitor voltage and the currents flowing through the shoot-through inductors. Notably, the flying capacitor voltage was balanced at around 200 V with considerably small peak-to-peak ripples of 4.5 V (see Figure 6(a)). Additionally, the currents flowing through shoot-through inductors (see Figure 6(b)) depict unipolarity, which is the critical characteristic for the dual-buck inverter to suppress shoot-through problems because the current does not change polarity, unlike the conventional FC inverter.

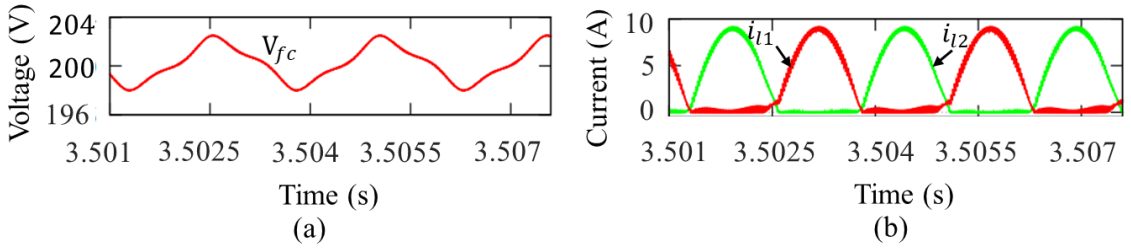

Figure 6: Simulated (a) flying capacitor voltage and (b) shoot-through inductor currents of the novel dual-buck FC inverter.

The current stresses in the MOSFETs of the conventional FC and novel dual-buck

inverters were analyzed at unity power factor, as shown in Figure 7. Comparing the drain currents flowing through the switches in both inverter topologies, all currents in the novel dual-buck inverter are uni-directional, unlike in the conventional FC inverter in which the current flowing through Q_2 and Q_4 have both positive and negative polarities (c.f. Figure 7(a) and (b)). Moreover, the current stresses in the dual-buck inverter were considerably reduced in the switches Q_2 and Q_4 (c.f. Figure 7(a) and (b)). These results confirm that the reliability of the dual-buck inverter has been improved, and the crosstalk effects are mitigated.

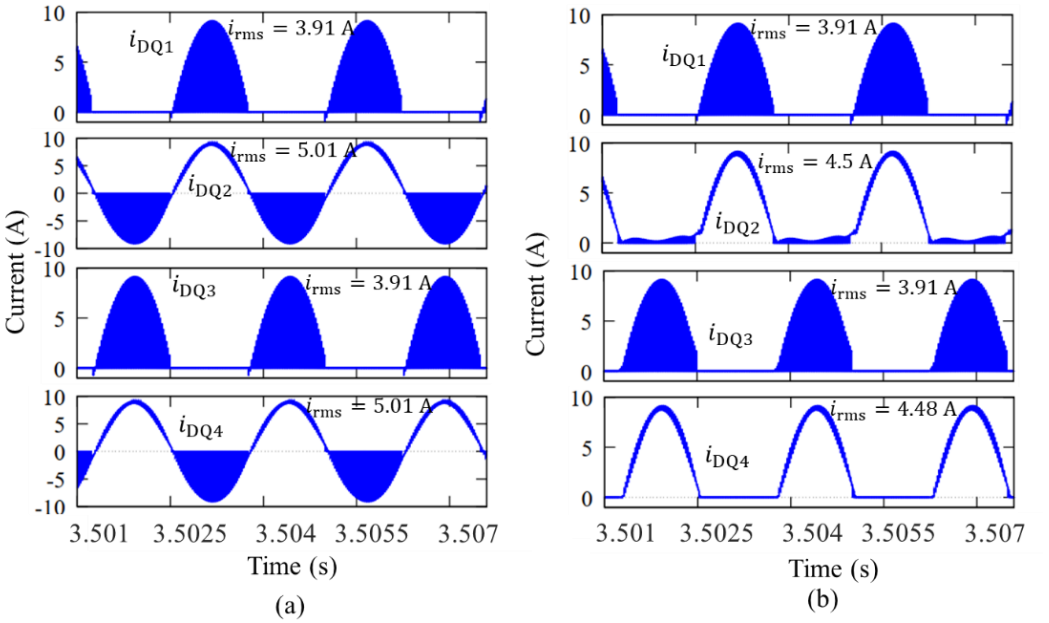

Figure 7: Drain currents flowing through MOSFETs of the (a) conventional FC inverter and (b) novel dual-buck FC inverter at unity power factor.

Figure 8 shows the current flowing the SiC diodes of the novel dual-buck inverter. Despite the novel dual-buck FC inverter having additional diodes, unlike the conventional FC inverter, it can be seen that the current stress in the diodes is small compared to other switches. Consequently, the increased power loss in these diodes is considerably small (i.e., 5% and 0.0% of the total power loss for D_2 and D_1, respectively). It is worth mentioning that the current stress in these diodes may change based on the operating power factor.

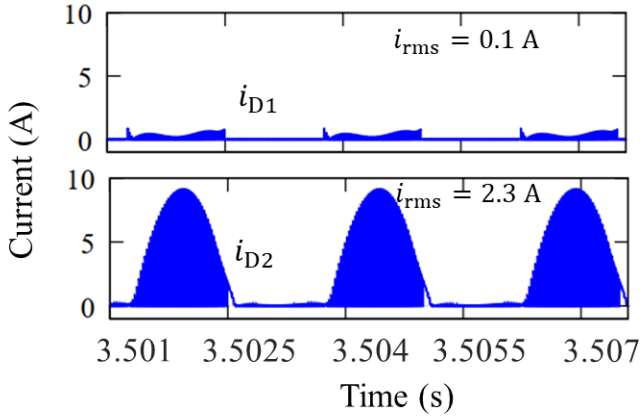

Figure 8: Currents flowing through SiC diodes of the novel dual-buck FC inverter at unity power factor.

A Fast Fourier analysis was performed on the output current to determine its total harmonic distortion (THD) with the output power variation in both inverters to confirm the higher waveform purity in the novel dual-buck FC inverter than in the conventional FC inverter. The inverters with a maximum output power of 785 W were simulated in the PLECS software. Comparing the THD trends in both inverter topologies, the novel dual-buck FC inverter achieves lower THD values at all output powers than the conventional FC inverter (see Figure 9). Specifically, the novel dual-buck FC inverter achieves 1% lower THD than the conventional FC inverter at the rated output power.

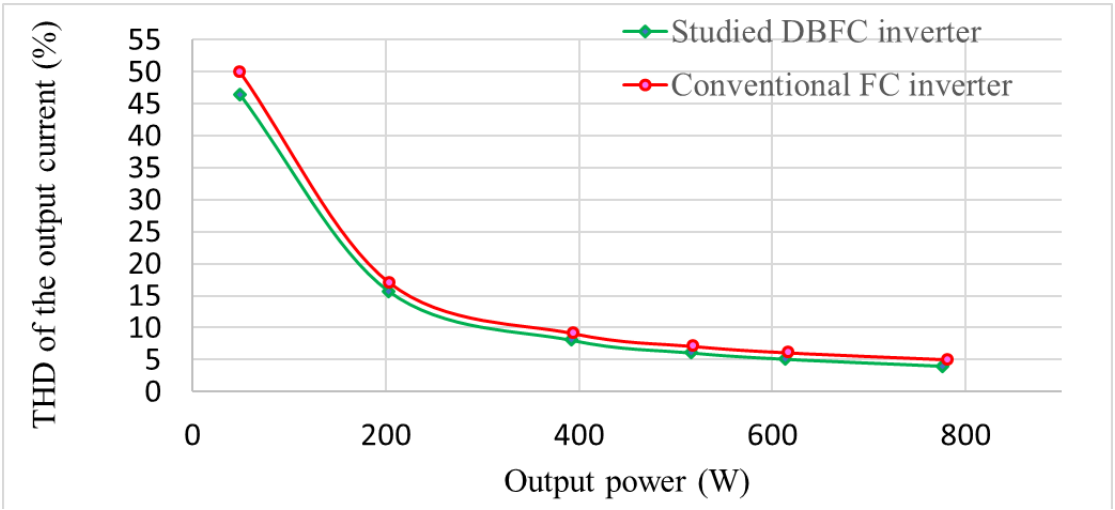

Figure 9: Total harmonic distortion of the output current with the output power variation.

Furthermore, the efficiency analysis of the novel dual-buck FC and conventional FC inverters was conducted in PLECS software using a model rated at 785 W. It was observed that the DBFC inverter achieves a maximum of 98.77% at a switching frequency of 40 kHz when the output power is 203 W. The efficiency of the DBFC inverter at the rated output power was 97.74%. It is worth mentioning that the efficiency of the DBFC inverter improves as the switching frequency decreases because most of the power losses are due to switching losses. However, an optimal switching frequency selection is necessary to achieve a balanced ratio between the inverter's power loss and power density (Mushi et al., 2017). On the other hand, it was observed that the conventional FC inverter achieved a slightly higher efficiency (98.92% at the output power of 203 W) than the DBFC because of the absence of shoot-through inductors in the conventional FC inverter.

The simulation analysis depicts that the novel three-level dual-buck FC inverter mitigates crosstalk effects, and the switches experience reduced current and voltage stress compared to the conventional topology. Moreover, the output power quality improves in the novel topology compared to the traditional inverter under similar dead time conditions.

Experimental results

An experimental prototype of the novel dual-buck three-level FC inverter shown in Figure 2 was constructed in the laboratory using four SiC MOSFETs and two Schottky diodes. The circuit parameters are similar to the one in the simulation except for the DC source voltage and load resistor, which were changed to 160 V and 9 Ω, respectively. The switching signals for the switches were realized using on-board Cyclone IV E FPGA.

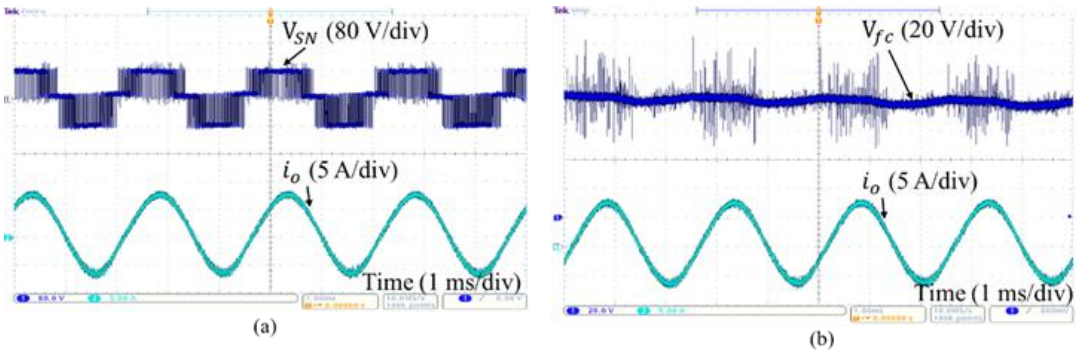

Figure 10: Experimental results of (a) output voltage and current and (b) flying capacitor voltage and output current obtained in the single-phase three-level dual-buck FC inverter.

Figure 10 depicts the steady-state experimental results of the output voltage, output current, and the flying capacitor voltage. Notably, the novel dual-buck FC inverter generates three voltage levels of magnitude 80, 0, and -80 V (see Figure 10(a)), verifying the theoretical and simulation analyses, as demonstrated in Figure 5(a). Moreover, the inverter's output current is almost pure sinusoidal with slight distortions, verifying the simulation result in Figure 5(b). Additionally, under the adopted modulation strategy, the flying capacitor voltage was well balanced at around 80 V (see Figure 10(b)), confirming the applied method's effectiveness.

CONCLUSIONS

This paper studied a novel three-level dual-buck flying capacitor inverter. The inverter was constructed in such a way as to suppress the shoot-through problems that may occur because of crosstalk effects, as exhibited in the traditional FC inverter. The detailed operation of the DBFC inverter was performed using a comparative analysis of the conventional FC inverter as a benchmark. It was noted that the DBFC inverter considerably reduces the current stress on some switches and mitigates the shoot-through problem. The novel DBFC inverter also reduced the THD of output current (1% lower at the rated output power) compared to the traditional FC inverter. Moreover, the novel dual-buck inverter achieved a maximum simulated efficiency of 98.8% at a switching frequency of 40 kHz. On the other hand, the conventional FC inverter achieved a slightly higher efficiency of 98.9%. In the future, the optimal short-circuit inductor design is necessary to reduce power loss in the inductor coil.

ACKNOWLEDGMENT

Authors express gratitude to Prof. Yasutaka Fujimoto of Yokohama National University, who assisted during the construction of the three-level dual-buck inverter prototype.

REFERENCES

Calderon-Lopez, G., Todd, R., Forsyth, A.J., Wang, J., Wang, W., Yuan, X., Aldhaher, S., Kwan, C., Yates, D., & Mitcheson, P.D. (2020). Towards lightweight magnetic components for converters with wide-bandgap devices. *Energy Conversion Congress Exposition Asia (IPEMC2020-ECCE Asia)*: 1–6.

Ebersberger, J., Hagedorn, M., Lorenz, M., & Mertens, A. (2022). Potentials and comparison of inverter topologies for future all-electric aircraft propulsion. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 10(5)*: 5264–5 279.

Faraji, F., Ghias, A.M.Y., Guo, X., Chen, Z., Lu, Z., & Hua, C. (2023). A split-inductor flying capacitor converter for medium-voltage application. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 11(1)*: 754–774.

Kahwa, A. and Mushi, A.T. (2024). Analysis of an Improved Reliability Dual-Buck Structured Three-Level Flying Capacitor Inverter. *8th International Conference on Mechanical and Industrial Engineering*. Arusha.

Kahwa, A., Obara, H., & Fujimoto, Y. (2018). Design of 5-level reduced switches count H-bridge multilevel inverter. *2018 IEEE 15th International Workshop on Advanced Motion Control (AMC)*: 41–46.

Khan, A.A., Cha, H., & Lai, J.-S. (2018). Cascaded dual-buck inverter with reduced number of inductors. *IEEE Transactions on Power Electronics, 33(4):* 2847–2856.

Liu, M., Hong, F., & Wang, C.H. (2013). A Novel flying-capacitor dual buck three-level inverter. *28th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*: 502–506).

Liu, M., Hong, F., & Wang, C.H. (2016). A Novel five-level flying-capacitor dual buck inverter. *Journal of Power Electronics, 16(1)*: 133–141.

Mushi, A., Nagai, H.., Obara, H., & Kawamura, A. (2017). Design for nonlinear current reference deadbeat control for boost converter. *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia)*: *665–670.*

Ning, J., Ben, H., Li, J., Wang, X., & Meng, T. (2024). A small-sized high-precision digital closed-loop modulation method for dead-time compensation for flying capacitor three-level inverters. *IEEE Transactions on Power Electronics, 39(4)*: 3968–3973.

Pahlevani, M., & Jain, P.K. (2020). Soft-switching power electronics technology for electric vehicles: A technology review. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 1(1)*: 80–90.

Shukla, A., Ghosh, A., & Joshi, A. (2007). Capacitor voltage balancing schemes in flying capacitor multilevel inverters. *Power Electronics Specialists Conference*: 2367–2372.

Yao, Z. (2021). Review of dual-buck-type single-phase grid-connected inverters. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 9(4)*: 4533–4545.

Yuan, X., Laird, I., & Welder, S. (2021). Opportunities, challenges, and potential solutions in the application of fast-switching SiC power devices and converters. *IEEE Transactions on Power Electronics, 36(4)*: 3925–3945.